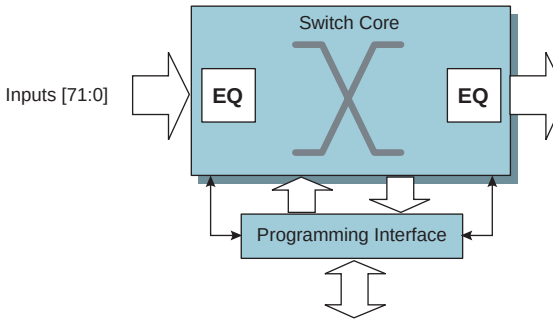
BLOCK DIAGRAM:



FEATURES:	BENEFITS:
6.5 Gbps 72 × 72 strictly nonblocking switch matrix with multicast and output striping programming modes	468-Gbps aggregate bandwidth in a single chip for storage, FC, blade server, and Ethernet systems
Fourth-generation input signal equalization (ISE) with programmable control globally or on a per-channel basis	Addresses system-level and board-level signal integ intersymbol interface (ISI) jitter issues
Adjustable output pre-emphasis EQ	EQ and drive flexibility for driving boards, cables, ar
Differential current mode logic (CML) data output driver	Convenient I/O flexibility for interfacing with multiple
Protocol-independent switching and data transmission	Can be used with latest storage, Ethernet, and netw
10-W typical power dissipation	Low 140-mW per-channel power dissipation
33 mm × 33 mm, 1.27 mm pin pitch, 613-pin FCBGA package	Layout-friendly package and pinout for easier PCB
Parallel and serial programming modes for configuration and monitoring	Programming and control convenience
Software control to optimize power dissipation	Controlled power reduction for unused ports

APPLICATIONS:

- Core and metro transport
- Enterprise
- Blade servers
- High-speed automated test equipment
- Broadcast video systems
- Storage, Ethernet, and networking equipment

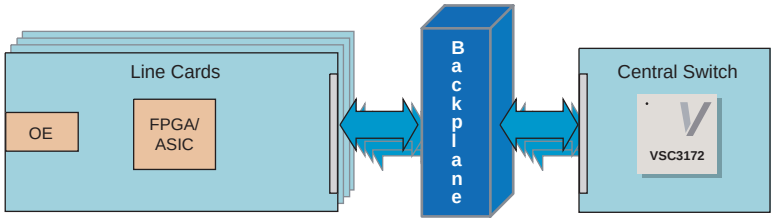
through a multimode port interface that allows random access programming of each input and output port.

A high degree of signal integrity is maintained throughout the device by fully differential signal paths. Programmable input EQ and output pre-emphasis settings enable maximum customization for the application. Each data output can be programmed to connect to one of the inputs. The signal path is unregistered and fully asynchronous, so there are no restrictions on the phase, frequency, or signal pattern on any input.

multiplexed parallel data. Core programming port-by-port basis, or multiple program assignm issued simultaneously.

Unused channels may be powered down to switch in applications that require only a Power-down is enabled in software by progra outputs with a power-down code.

BACKPLANE APPLICATION:



SPECIFICATIONS:

- 6.5-Gbps NRZ per-channel data rate
- 2.5-V power supply (2.5-V or 3.3-V program port power supply)
- 2.5-V or 3.3-V CMOS TTL-compatible I/O
- Differential CML I/O with integrated termination impedance
- 0 °C to 85 °C operating temperature range

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